## **CLAIMS**

## We claim:

1	1. A method of extracting electrical characteristics from an integrated
2	circuit layout, said method comprising:
3	dividing said integrated circuit layout into at least one extraction sub problem;
4	identifying a set of physical parameters that define said extraction sub problem
5	from said integrated circuit layout;
6	supplying said set of physical parameters to a machine-learning model trained
7 -	with Bayesian inference implemented with a Monte Carlo method; and
8	calculating at least one electrical characteristic for said extraction sub problem by
9	analyzing said set of physical parameters with said machine-learning model
10	trained with Bayesian inference implemented with a Monte Carlo method.
1	2. The method as claimed in claim 1 wherein said electrical
2	characteristic comprises capacitance.

- 1 3. The method as claimed in claim 1 wherein said electrical characteristic comprises resistance.
- 1 4. The method as claimed in claim 1 wherein said extraction sub 2 problem comprises a net.

DHJ --56-- SPLX.P0061

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physical parameters comprises a wire length.

2	problem comprises a section of interconnect wiring.
1	6. The method as claimed in claim 1 wherein one of said set of
2	physical parameters comprises a distance between a pair of interconnect lines.
1	7. The method as claimed in claim 1 wherein one of said set of
2	physical parameters comprises a wire width.
1	8. The method as claimed in claim 1 wherein one of said set of

The method as claimed in claim 1 wherein said extraction sub

1 9. The method as claimed in claim 1, said method further comprising:

2 selecting said machine-learning model from a plurality of machine-learning

3 models.

DHJ --57-- SPLX.P0061

	10. The method as claimed in claim I wherein calculating at least one			
electrical characteristic for said extraction sub problem comprises:				
	determining a capacitance per unit length for a subsection of interconnect wiring			
	and			
	multiplying said capacitance per unit length by a length of said subsection of			
	interconnect wiring.			

comprising an arranged set of computer instructions for:

dividing an integrated circuit layout into at least one extraction sub problem;
identifying a set of physical parameters that define said extraction sub problem
from said integrated circuit layout;
supplying said set of physical parameters to a machine-learning model trained
with Bayesian inference implemented with a Monte Carlo method; and
calculating at least one electrical characteristic for said extraction sub problem by
analyzing said set of physical parameters with said machine-learning model
trained with Bayesian inference implemented with a Monte Carlo method.

12. The computer readable medium as claimed in claim 11 wherein said electrical characteristic comprises capacitance.

DHJ --58-- SPLX.P0061

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2	said electrical characteristic comprises resistance.	
1 2	14. The computer readable medium as claimed in claim 11 wherein said extraction sub problem comprises a net.	
1 2	15. The computer readable medium as claimed in claim 11 wherein said extraction sub problem comprises a section of interconnect wiring.	
1 2 3	16. The computer readable medium as claimed in claim 11 wherein one of said set of physical parameters comprises a distance between a pair of interconn lines.	.ec
1 2	17. The computer readable medium as claimed in claim 11 wherein one of said set of physical parameters comprises a wire width.	
1	18. The method as claimed in claim 1 wherein one of said set of	

The computer readable medium as claimed in claim 11 wherein

DHJ --59-- SPLX.P0061

physical parameters comprises a wire length.

1	19.	The computer readable medium as claimed in claim 11 wherein
2	said arranged set of computer instructions further perform:	
3	selecting said	l extraction sub problem model from a plurality of extraction sub
4	problem 1	models.

20.	The computer readable medium as claimed in claim 11 wherein a			
subset of compute	instructions for calculating at least one electrical characteristic for			
said extraction sub problem perform the follow:				
determining a capacitance per unit length for a subsection of interconnect				
and				
multiplying	g said capacitance per unit length by a length of said subsection of			
interco	nnect wiring.			

DHJ --60-- SPLX.P0061